

**Amendments to the Specification:**

On page 1, after the title and before the background section, please insert the following:

**-- CROSS-REFERENCES TO RELATED APPLICATIONS**

This is a Divisional Application of U.S. Patent Application No. 09/895,579, filed June 29, 2001. This Divisional Application claims the benefit of the U.S. Patent Application No. 09/895,579. –

Please replace the heading on page 1, line 6, with the following rewritten heading:

**-- DESCRIPTION OF THE RELATED ART –**

Please replace the paragraph beginning on page 3, line 11, with the following rewritten paragraph:

-- The relaxed SiGe layer 102 is formed upon or deposited on top the silicon substrate 101. The strained silicon layer 104 is then formed on the relaxed SiGe layer 102. In one embodiment, the relaxed SiGe layer 102, and the strained silicon layer 104 are formed by an epitaxial growth process. In other words, the process includes epitaxial growth of relaxed SiGe on the silicon wafer 101 to create the relaxed SiGe layer 102, epitaxial growth of a thin silicon film on the stack structure of the silicon wafer 101 to create the strained silicon film 104. The relaxed SiGe layer has the thickness in the range of approximately from 0.1 $\mu$ m to 3.0 $\mu$ m. It is contemplated that the forming of these layers in the stack structure may be done in any other process other than the epitaxial growth process.--

Please replace the paragraph beginning on page 4, line 27, with the following rewritten paragraph:

-- Figure 6 is a diagram illustrating Figure 5 with further heat treatment to transfer the strained layer to the oxidized wafer according to one embodiment of the invention. After the lower heat treatment to result the bonding of silicon wafer 101 and oxidized wafer 401, higher temperature heat treatment is applied. This temperature used in this further heat treatment ranges from approximately 400 °C to 600 ° C. The higher temperature heat treatment results in the bonding of surface 104 to wafer 101 at the SiO<sub>2</sub> interface 601. The further heat treatment also results in the separation of the two wafers at the embrittled region (described in Figure 2). After

the further heat treatment, the two wafers 101 and 401 are delaminated along the embrittled implanted region (i.e., H-implanted SiGe region). This effectively separates the two wafers and the strained silicon film 104 is transferred to the SOI-like wafer 401. In one embodiment, the embrittled region resides on the relaxed SiGe layer 102. When the two wafers 101 and 401 separate, the strained silicon layer 104 and the part of the relaxed SiGe layer 102 are transferred to the SOI wafer 401. Part of relaxed SiGe layer 102 is then etched off to result the wafer 401 with the strained silicon layer 104 on top of the SiO<sub>2</sub> layer. This results in the transfer of the strained silicon layer 104 to the SOI wafer 401 (e.g., oxidized wafer 401). It is contemplated that the etching may be wet or plasma etching; however, wet etching is used to better remove the entire SiGe residue on the strained silicon film.--

Please replace the paragraph beginning on page 5, line 14, with the following rewritten paragraph:

-- In one embodiment where there is no implanting step (i.e., hydrogen implant), the embrittled region is not formed. The strained silicon layer 104 is transferred to the SOI wafer 401 by a bonded-etchback process on the silicon wafer 101 and the strained SiGe 104. this gives the strained silicon film on the SOI wafer 401.--